ELLIOTT 403 - WREDAC

(Weapons Research Establishment Digital Automatic Computer)

The following 36 pages (except for the title page which is reproduced as a photo-copy of the original), are a re-typed version of a manual written by D. L. Overheu, called "An introductory coding manual for the WRE digital automatic computer". The manual is undated, but was probably written in 1959 or 1960, and was produced by the Department of Supply - Weapons Research Establishment, in Australia.   A copy of this manual is to be lodged in the London Science Museum.

D.J.P

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AN INTRODUCTORY CODING MANUAL FOR THE

WRE DIGITAL AUTOMATIC COMPUTER

by

D.L. Overheu

PRECIS

An elementary Coding Manual for the WREDAC has been constructed in order to assist those who wish to learn the WREDAC coding. It is also intended as a reference to the present state of orders and coding for the WREDAC.

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1. INTRODUCTION

Since the writing of Programming Memo No.1 (1) a considerable number of changes have been made to the WREDAC. Further, TM50 (2) is now so out of date as to be very nearly useless as a reference for machine coding. This Tech. Memo will bring together in one place a number of useful Programming and Operating Memoranda at present in existence (3), (4) so that programmers and coders will have an immediate reference available. It will also supersede several previous Operating and Programming Memoranda (5) (6) (7) (8).

2. THE WREDAC

The digital computer operates in the serial binary mode with 34 digits to a number word. The negative of a number is represented by the 2's complement of the number. Hence, the most significant digit will be a one for a negative number and the machine will have 33 effective digits in the word.

Owing to the method of multiplication and division employed in the machine, it is convenient to regard these 33 digits as having 32 digits after the binary point. Thus the machine may be regarded as being able to represent all numbers in the range $-2 <= x <= 2^{-32}$ which differ by integral multiples of 2^{-32}. It is important to remember this restriction when numbers are entered into the machine for computation.

There are three levels of addressable word storage available in the machine. The first of these is termed the high speed store and consists of 127 delay lines each of four word capacity, 12 delay lines each of one word capacity, and a set of console keys called the number generator. The high speed store is arranged in 8 blocks, each of 64 words, plus an additional set of 9 single word stores; each word of the high speed store is individually addressable, although addressing one of the 12 single word lines may need to be preceded by a special machine order which is discussed in paragraphs 3.6.1 and 3.6.2.

The second level of addressable storage is a rotating magnetic disc storing 16,384 words on 64 tracks each of which stores 256 words. Each track is divided into four sectors each storing 64 words. Thus a sector of 64 words (see paragraph 4.2.1) is equivalent to a block of high speed store. A block of 64 words only may be transferred to the high speed store at a time, i.e. individual words are not addressable on the disc. It is convenient, therefore, to regard the disc as having the equivalent of 256 addressable sectors, or 'blocks' each of 64 words.

The third level of addressable storage consists of up to four magnetic tape units. These units use ½"[1/2 inch] magnetic tape and store the 34 digits of a word in six rows of six digits each. This store is made addressable by virtue of the ability to nominate the tape unit to be used and by previous writing, under machine control, of known marker words on the tape. There are three main modes for the operation of the tape units as backing stores. Single words can be written in records of variable length with a particular word acting as the marker, blocks of 64 words can be written with some word within the block acting as the marker (the usual mode) or blocks of 64 words can be written with single words between blocks acting as the markers.

The Arithmetic Unit of the machine contains a double length accumulator of 68 digits. The most significant 34 digits of the accumulator are referred to as the 'upper half accumulator', and the least significant 34 digits as the 'lower half accumulator'. Most arithmetic and logical operations take place through the accumulator, but the accumulator is not directly addressable. The result of a multiplication or division is formed in the accumulator, and a separate store called the 'multiplier register' is used to hold one term of the arithmetic operation (the multiplier or divisor) during the process of multiplication or division. The multiplier register is not addressable.

The Control Unit which directs the automatic operation of the machine has four single word stores, which are known collectively as the 'order store', and a halfword delay line termed an 'order register'. The order store is refilled after the instructions contained in four words have been obeyed. The order register always contains the current instruction to be obeyed.

The machine has high-speed photo-electric paper tape readers using five hole punched paper teletape for input, and five hole paper tape punches for output. In addition, the magnetic tape units are a form of high speed input/output when not in use as addressable stores.

The instruction or order code of the WREDAC for arithmetic and logical operations is the single address type specifying a function, a high speed store address, and a B-line or indexing register. There are 32 arithmetical and logical functions known as '0-Code' orders and 32 inter-store transfer and control functions known as '1-Code' orders. The instruction word consists of 17 digits so that two instruction words are contained in a machine word of 34 digits. The format of the 0-Code instruction word is indicated in the following diagram:

	Function digit	Address digits		B-line digits	Code digit	
Most Significant Digit	34 33 32 31 30	29 to 21		20 19	18	Least Significant Digit
	17 16 15 14 13	12 to 4		3 2	1	
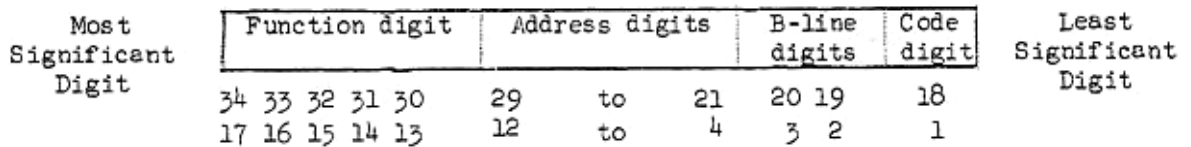
Thus, there are five digits for functions, nine for address, two for B-lines, and one for the code digit. The format of the 1-Code instruction word at present varies with the type of instruction.

A list of abbreviations which will be used throughout the remainder of this memorandum will be found in Appendix I.

3.   0-CODE ORDERS

The 0-Code orders are specified by a zero digit in the least significant position of the instruction word. This digit directs the machine to perform some arithmetic or logical function.

A list of 0-Code orders is given in Appendix II together with other relevant information for ready reference. In the following brief description of each function, the 'odd half' and 'even half' of a high speed store location or address are the most significant and least significant 17 digits respectively. The orders are obeyed serially in the sequence x even, x odd, (x+1) even, (x+1) odd etc., where x is the high speed store address of the current order.

3.1   Transfers of Control
There are five control transfer orders which are conditional upon the contents of the accumulator, and one unconditional transfer of control order. The machine binary code and mnemonic code is given below for each of these orders.

3.1.1 The Order CH (CHECK)

34		18
17		1
0 0 0 0 0	ADDRESS A	00	0
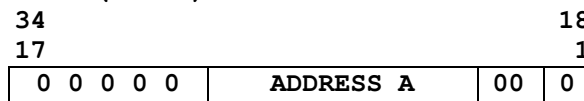
1. If A = 0, no effect
2. If A not = 0, transfer control to the order in the
    odd half of address A if and only if (Acc) = 0,
    otherwise proceed sequentially.
NOTE that the whole of the double length accumulator
is tested by this order so that a control transfer will
not occur if the lower half accumulator is not zero.

3.1.2 The Order GE (GO EVEN)

34		18
17		1
0 0 0 0 1	ADDRESS A	00	0

Transfer control unconditionally to the order in the even half of address A. The accumulator is not altered by this order.

3.1.3 The Order PO (POSITIVE ODD)

34		18
17		1
0 0 0 1 0	ADDRESS A	00	0

Transfer control to the order in the odd half of address A if (Acc) >= 0, otherwise proceed sequentially. Hence the most significant (34th) digit of a word in the accumulator will be zero if control is transferred. The accumulator is not altered by this order.

3.1.4 The Order PE (POSITIVE EVEN)

34		18
17		1
0 0 0 1 1	ADDRESS A	00	0

Transfer control to the order in the even half of address A if (Acc) >= 0, otherwise proceed sequentially. The accumulator is not altered by this order.

3.1.5 The Order NO (NEGATIVE ODD)

34		18
17		1
0 0 1 0 0	ADDRESS A	00	0

Transfer control to the order in the odd half of address A if (Acc) < 0, otherwise proceed sequentially. Hence the most significant digit of the Accumulator will be a one if control is transferred. The accumulator is not altered by this order.

3.1.6 The Order NE (NEGATIVE EVEN)

34		18
17		1
0 0 1 0 1	ADDRESS A	00	0

Transfer control to the order in the even half of address A if (Acc) < 0,otherwise proceed sequentially. The accumulator is not altered by this order.

3.2 Orders for information transfer

There are six machine orders for transferring or exchanging information within the high speed store. Five of these orders involve the accumulator directly.

3.2.1 The Order SM (SET MULTIPLIER)

```
34                                    18
17                                     1
| 0 1 0 0 1 |   ADDRESS A   | 00 | 0 |
```

Transfer the contents of address A to the multiplier register.
The number in addressed store A is not affected by this order and the
content of the multiplier register is replaced by the content of A.

The multiplier register, R, is not addressable, and this order
is the only means by which numbers can be transferred to R. It
is not possible to transfer a number directly from the
accumulator to R since the accumulator is also not addressable.

3.2.2 The Order SW (SWAP)

```
34                                    18
17                                     1
| 1 0 0 1 0 |   ADDRESS A   | 00 | 0 |
```

Exchange the contents of the upper half accumulator with the
contents of high speed store address A. The lower half of the
accumulator is set to zero by this order.

3.2.3 The Order CL (CLEAR)

```
34                                    18
17                                     1
| 1 0 0 1 1 |   ADDRESS A   | 00 | 0 |
```

Transfer the contents of the upper half accumulator to the high
speed store address A and set the accumulator to zero. Both
the upper and lower halves of the accumulator are set to zero.

3.2.4 The Order CO (CLEAR TO ODD)

```
34                                    18
17                                     1
| 1 1 0 0 1 |   ADDRESS A   | 00 | 0 |
```

Transfer the 17 most significant digits (i.e. digits 34 to 18) of
the accumulator to the odd half (i.e. most significant half) of the
high speed store Address A and set the accumulator to zero. Both
the upper and lower halves of the accumulator are set to zero.

3.2.5 The Order CE (CLEAR TO EVEN)

```
34                                    18
17                                     1
| 1 1 0 1 0 |   ADDRESS A   | 00 | 0 |
```

Transfer the 17 most significant digits of the accumulator to
the even half (i.e. least significant half) of the high speed
store address A and set the accumulator to zero. Both the upper
and lower halves of the accumulator are set to zero.

3.2.6 The Order ST (STORE)

34		18
17		1
1 1 0 1 1	ADDRESS A	00	0

Transfer the contents of the upper half accumulator to the high
speed store address A without changing the contents of the
accumulator.

3.3 Arithmetic Orders

There are fifteen orders for arithmetic operations. Six of
these orders are concerned with multiplication and division, four
are concerned with addition and subtraction, one with obtaining
the absolute value of a number, and four affect only the most or
least significant 17 digits of a word.

3.3.1 The Order LD (LONG DIVISION)

34		18
17		1
0 1 0 0 0	ADDRESS A	00	0

The number in high speed store address A is divided by the
number in the multiplier register R and the 34 digit result is
added to the accumulator, the number in the high speed store
address A is not altered. Hence, the multiplier register must
be set by an SM order before division and the accumulator must
be cleared unless accumulation is required. The result x of a
division must lie in the range $-2 < x <= 2 - 2^{-32}$.

3.3.2 The Order MA (MULTIPLY and ADD)

34		18
17		1
0 1 0 1 0	ADDRESS A	00	0

The number in high speed store address A is multiplied by the
number in the multiplier register R and the 66 digit product is
added to the accumulator. The number in the high speed store
address A is not altered. The product will occupy both the
upper and lower halves of the accumulator. The multiplier
register must be set by an SM order before the multiplication
order is obeyed and the accumulator cleared, unless
accumulation is required. The product must lie in the range
$-2 < x <= 2 - 2^{-64}$.

3.3.3 The Order MS (MULTIPLY and SUBTRACT)

34		18
17		1
0 1 0 1 1	ADDRESS A	00	0

As for the MA order except that the product is subtracted from
the accumulator.

3.3.4 The Order SL (SHIFT LEFT)

34		18
17		1
0 1 1 0 0	NUMBER OF SHIFTS N	00	0

The number in the accumulator is multiplied by 2^N where N is specified by the address part of the order. Since N is reduced by unity until it becomes zero in the Control Unit, multiplication by 2^N takes N times the time to perform a multiplication by 2 using the SL order. If N > 68, the accumulator will be cleared to zero, i.e. 'end round' shift does not occur. If the accumulator is zero, the machine will still obey the SL order N times before stepping to the next order.

3.3.5 The Order SR (SHIFT RIGHT)

34		18
17		1
0 1 1 0 1	NUMBER OF SHIFTS N	00	0

The number in the accumulator is multiplied by 2^{-N} where N is specified by the address part of the order. In operation, N is reduced by unity, in the Control Unit until it becomes zero, so that multiplication by 2^{-N} takes N times the time to perform a multiplication by 2^{-1} using the SR order. If the number in the accumulator is positive and N > 68, the accumulator will be cleared to zero. If the number in the accumulator is negative, a one will be entered in the most significant digit position of the accumulator each time a right shift of one binary place occurs. Hence if N > 68, the accumulator will be set to -2^{-66}.

3.3.6 The Order NM (NORMALISE)

34		18
17		1
0 1 1 1 0	NO ADDRESS	00	0

The accumulator is subjected to left shifting until $1 <= |(Acc)| < 2$, i.e. the accumulator is multiplied by 2^M. The number of left shifts M, (i.e. the power of 2 necessary) is automatically counted in a machine B-line in the form $M \times 2^{-29}$. The 34 digits of the B-line will be set to zero before commencing the count.
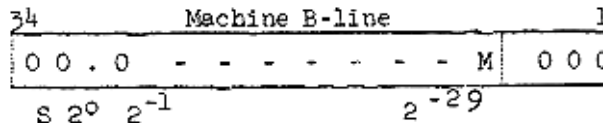
If the accumulator is already normalised, −2, or zero, the NM order has no effect, except that the B-line is set to zero.

3.3.7 The Order MD (MODULISE)

```
34                                    18
17                                     1
| 0 1 1 1 1 |     NO ADDRESS     | 00 | 0 |
```

If the number in the accumulator is negative make it positive, i.e. change the number in the accumulator to its absolute value. Note that −2 will not become zero, but will remain −2.

3.3.8 The Order CA (CLEAR and ADD)

```
34                                    18
17                                     1
| 1 0 0 0 0 |     ADDRESS A     | 00 | 0 |
```

Set the accumulator to zero and add the number in high speed store address A to the accumulator. The number in the high speed store address A is not changed.

3.3.9 The Order CS (CLEAR and SUBTRACT)

```
34                                    18
17                                     1
| 1 0 0 0 1 |     ADDRESS A     | 00 | 0 |
```

Set the accumulator to zero and subtract the number in high speed store address A from the accumulator. The number in the high speed store address A is not altered.

3.3.10 The Order AD (ADD)

```
34                                    18
17                                     1
| 1 0 1 0 0 |     ADDRESS A     | 00 | 0 |
```

Add the number in high speed store address A to the number in the accumulator. The number in high speed store address A is not altered.

3.3.11 The Order SA (SUBTRACT and ADD)

```
34                                    18
17                                     1
| 1 0 1 0 1 |     ADDRESS A     | 00 | 0 |
```

Subtract the number in high speed store address A from the number in the accumulator. The number in high speed store address A is not altered.

3.3.12 The Order AO (ADD ODD)

```
34                                    18
17                                     1
| 1 1 1 0 0 |     ADDRESS A     | 00 | 0 |
```

Add the number in the odd (i.e. most significant) half of high speed store address A to the most significant half of the upper half of the accumulator. Thus, the number from digit positions 34 to 18 inclusive will be added to the accumulator in digit positions 34 to 18 inclusive. The high speed store address A is not altered, and the remainder of the accumulator will not be affected.

3.3.13 The Order SO (SUBTRACT ODD)

34			18
17			1
1 1 1 0 1	ADDRESS A	00	0

Subtract the odd (i.e. most significant) half of the number in
high speed store address A from the most significant half of
the upper half of the accumulator. The number in high speed
store address A is not altered and the remainder of the
accumulator is not affected.

3.3.14 The Order AE (ADD EVEN)

34			18
17			1
1 1 1 1 0	ADDRESS A	00	0

Add the even (i.e. .least significant) half of the number in
high speed store address A to the most significant half of the
upper half of the accumulator, i.e. add the number in digit
positions 17 to 1 inclusive of high speed store address A to
digit positions 34 to 18 inclusive of the accumulator. The
number in high speed store address A is not altered and the
remainder of the accumulator is not affected.

3.3.15 The Order SE (SUBTRACT EVEN)

34			18
17			1
1 1 1 1 1	ADDRESS A	00	0

Subtract the order in the even (i.e. least significant) half of
high speed store address A from the most significant half of
the upper half of the accumulator. The number in high speed
store address A is not altered and the remainder of the
accumulator is not affected.

3.4 Logical Functions

There is only one machine order for symbolic logical
functions. It is equivalent to the logical product or
intersection of two sets of entities. It can be used to select
binary digits from any position of a word by appropriate choice
of the word used for this selection.

3.4.1 The Order CT (COLLATE)

34			18
17			1
1 0 1 1 0	ADDRESS A	00	0

Compare the number in high speed store address A with the
number in the accumulator and leave 1's in the accumulator
digit positions which correspond with 1's in the equivalent
digit positions of the number in address A, but set accumulator
digit positions to zero which correspond to zeros in the
equivalent digit positions of the number in address A.

```
                          34
Example:         If (A) = 0 1 1 0 1 0 1 1 1 1 1 0 0 - - - - -
                (Acc) = 1 1 0 1 1 0 1 1 0 0 1 1 0 - - - - -
Then the CT order will
cause (Acc) to change to    0 1 0 0 1 0 1 1 0 0 1 0 0 - - - - -
```
The lower half of the accumulator will be set to zero.

3.5 Machine B−Line Orders

As mentioned earlier, the machine has 12 single word stores which may be used either as normal stores or for special purposes. These single word stores are normally referred to as 'B−lines', although, in general, only the even half of a single word store is involved in an operation which requires the use of a B−line. There are, however, three machine orders which require a whole single word store if they are to operate effectively. These orders allow a B−line to be set with a positive or negative number, and provide transfer of control and counting facilities, depending on the state of the B−line in use.

The method of switching these orders between B−lines is given in paragraph 3.6.1.

3.5.1 The Order SB (SET B−LINE)

34		18
17		1

1 1 0 0 0	A NUMBER 'A'	00	0

1. If $0 <= A <= 255$ then store this number as $n \times 2^{-29}$, where $n = A$, in the appropriate B−line, i.e. A appears as an integral binary number in the even half of the B−line with its units digit in digit position 4, and the odd half of the B−line is made zero.

2. If $256 <= A <= 511$, then store this number as $-n \times 2^{-29}$, where $512 - n = A$, in the appropriate B−line, i.e. A appears as an integral binary number in the address part of the even half of the B−line with units digit in digit position 4 and ones in all digit positions from 13 to 34 inclusive.

3.5.2 The Order JO (JUMP ODD)

34		18
17		1

0 0 1 1 0	ADDRESS A	00	0

1. If the B−line in use is not zero, transfer control to the order in the odd half of address A and add 1×2^{-29} to the B−line.
2. If the B−line in use is zero, proceed sequentially and add 1×2^{-29} to the B−line.
   NOTE that the content of B−line is tested <u>before</u> the addition takes place.

3.5.3 The Order JE (JUMP EVEN)

34		18
17		1

0 0 1 1 1	ADDRESS A	00	0

As for the order JO except that control may be transferred to the order in the even half of address A.

3.6 The order controlling machine operating mode.

One special order is reserved in the 0−code orders to determine the mode of operation of the machine. Allowance has been made for up to 8 different modes of operation, each one of which may be subclassified in 64 ways. Only one mode has been attached to the machine to date, namely, the 'use B−lines' mode.

3.6.1 The Order UL (USE LOGIC)

34		29	27		18	
17		12	10		1	
1 0 1 1 1		0 0 1	ADDRESS A		00	0

The digits in digit positions 27 to 29 or 10 to 12 inclusive, specify the mode of operation. Since only the B-line mode is available at present, the code has been indicated above in the appropriate position. The address A may be further analysed as follows:

34			26	25	24 23	22 21		18
17			9	8	7 6	5 4		1
1 0 1 1 1		0 0 1					00	0

From the least significant end:

      digits 4, 5 specify the B-line to which the SB, JO, JE and NM orders apply

      digits 6, 7 specify the group of three B-lines, from the 4 available, which will be switched to high speed store addresses 1,2,3 respectively.

      digits 8, 9 specify the two B-lines which may be added together before being used as modifiers (see paragraph 3.6.2 below).

      Similarly, for digits 21 to 26.

Appendix IV gives further details of the use of this order. As an example, it is possible to nominate B-line 1 for the automatic counting facility and B-lines 2 and 3 to be additive only when B-line 3 is the modifying B-line.

3.6.2 Machine B-Lines

The machine B-lines consist of the even part of the 12 single word stores referred to in paragraphs 2, 3.3.5 and 3.3.6, together with a permanently zero B-line. Following a UL order referring to B-line usage, the group of 3 B-lines specified will effectively occupy addresses 1, 2 and 3 of the high speed store. Since zero address is the number generator, B-line 0 is never referred to in the address portion of an instruction. For convenience, the B-lines are given the Greek letters $\alpha, \beta, \gamma, \delta$. The diagrams below indicate the manner in which B-line digits of the instruction word are used to specify a given B-line.

	34			18	
	17			1	
B-line '0' or 'α'	FUNCTION	ADDRESS	0 0	0	
B-line '1' or 'β'	FUNCTION	ADDRESS	0 1	0	
B-line '2' or 'γ'	FUNCTION	ADDRESS	1 0	0	
B-line '3' or 'δ'	FUNCTION	ADDRESS	1 1	0	

An order specifying a B-line by the B-line digits of the order will cause the contents of at least one B-line (even half of α, β, γ or δ) to be added to the remaining more significant 14 digits of the order before the order is obeyed. Thus, it is important to note that when carrying out address modification, overflows from the address portion of the instruction will be added to the function digits thus possibly altering the intended meaning of the instruction.

It is also important to note that following certain UL orders, a given B-line digit specification will cause the sum of that B-line plus one other to be added to the order before it is obeyed. Thus, if the 6 least significant address digits of the UL order have the decimal significance 16 to 31, 32 to 47, or 48 to 63, the addition of β and γ, γ and δ, or δ and β, will occur before instruction modification when an instruction has β, γ or δ digits respectively in the B-line digits position of the instruction.

4.   1-CODE ORDERS

The 1-code orders are specified by a one digit in the least significant position of the instruction word. This digit specifies that the instruction will either cause the machine to perform some transfer of information between stores of different levels or between input/output equipment, or that the instruction will carry out some control operation of the peripheral equipment. 1-code orders cannot be modified by a B-line since some of these instructions require more address digits than the 0-code instructions. The majority of 1-code orders may be obeyed concurrently with subsequent 0-code orders, and any exceptions are noted below. On the other hand, the 0-code orders SL, SR and NM may be used to delay the operation of following 1-code orders until these shifting orders are completed. Appendix III contains an ordered list of 1-code instructions for ready reference.

4.1 Punched Paper Tape Input/Output Instructions
There are four instructions concerned with input and output of punched paper tape. These instructions all use the accumulator.

4.1.1 The Order IL (INPUT to LEAST)

34		18
17		1
0 0 0 1 0	NO ADDRESS	1

Read a row of teletape (5 hole punched paper tape) and add the digits read to the five least significant digits of the upper half of the accumulator; i.e. the digits read are added to the accumulator digits 1 to 5 inclusive. Note that the accumulator is not cleared before reading.

4.1.2 The Order IM (INPUT to MOST)

34		18
17		1
0 0 0 1 1	NO ADDRESS	1

Read a row of teletape and add the digits read to the five most significant digits of the accumulator, i.e. digits 30 to 34 inclusive. The accumulator is not cleared before reading.

4.1.3 The Order OL (OUTPUT from LEAST)

34		18
17		1
0 0 1 0 0	NO ADDRESS	1

Punch on teletape the five least significant digits of the upper half of the accumulator.

4.1.4 The Order OM (OUTPUT from MOST)

34		18
17		1
0 0 1 0 1	NO ADDRESS	1

Punch on teletape the five most significant digits of the accumulator.

4.2 Transfer of Information between High Speed Store and Magnetic Disc

Two orders are concerned with the transfer of numbers between the high speed store and the Magnetic Disc. As mentioned in paragraph 2, transfers must take place in blocks of 64 words. Since there are 8 blocks of high speed store and 256 blocks or 'sectors' of disc store, 11 digits are required to specify the addresses, 3 to specify the high speed store block and 8 to specify the disc sector. Transfers to the disc cannot take place concurrently with transfers from the disc.

4.2.1 The Order BD (BLOCK to DISC)

34	29	26	18
17	12	9	1
0 0 1 1 0	BLOCK ADDRESS	SECTOR ADDRESS	1

Transfer a block of 64 words from the high speed store block address given, to the disc sector address given. Any subsequent orders which do not involve high speed store block outputs will be performed during the transfer. Information in the block being transferred may also be used and could be affected during the transfer.

Note particularly that the <u>three least significant</u> digits of the <u>first word</u> of a block will always be zero when returned to high speed store from the disc. Hence care must be taken when numbers or programs are stored on disc so that this loss of digits does not affect the operation of a program.

4.2.2 The Order DB (DISC to BLOCK)

34	29	26	18
17	12	9	1
0 0 1 1 1	BLOCK ADDRESS	SECTOR ADDRESS	1

Transfer a block of 64 words from the disc sector address given to the block address given. Again, any orders not referring to the location in the block concerned, will be obeyed during the transfer. Those which do, and any high speed store block input orders, will not be obeyed until the transfer is completed.

4.3 Magnetic tape Orders

The remaining 1-code orders, except for one special order, are concerned with the control of magnetic tape units and the transfer of information between the high speed store, accumulator, and the magnetic tape. There are two independent control channels and a separate input and output channel.

In order to understand the following paragraphs it is necessary to anticipate some later paragraphs at this stage. The input of program to the machine requires the use of certain warning symbols on the paper tape.

Prior to the rearrangement of the 1-code functions and the introduction of independent control channels, these symbols used spare orders in the 1-code order structure. In order to retain the two-letter mnemonic code and to avoid major programming changes, it was decided to continue to write programs with magnetic tape orders in the same manner as before, with addresses, but to cause a machine program to alter these orders to the desired machine code. Hence the teletype characters punched for WT0 and WT1 orders, for example, are the same and the punching of a 0 or 1 in the address position causes the machine program to form the appropriate function character within the machine. The exception to this rule is the FG0, FG1 orders which must be separately punched with zero address.

4.3.1 Magnetic Tape Control Orders

Before the reading or writing of magnetic tapes can occur, the tape must be put into motion and positioned. There are eight 1-code orders for this purpose, four on control channel 0 and four on control channel 1. The following diagrams indicate how these orders would appear in the machine. Appendix III should be consulted to determine the correct method of punching the order on paper tape for input to the machine.

4.3.1.1 The Order TF0 (TAPE FORWARD)

34		18
17		1
1 1 0 0 0	NO ADDRESS	1

Run a tape unit connected to Channel 0 control forward. The forward motion of a tape occurs when the tape spools are rotating in a clockwise direction and tape is being fed from the upper spool to the lower spool.

4.3.1.2 The order TF1 (TAPE FORWARD)

34		18
17		1
1 1 0 0 1	NO ADDRESS	1

Run a tape unit connected to Channel 1 control forward.

4.3.1.3 The Order TR0 (TAPE REVERSE)

34		18
17		1
1 1 0 1 0	NO ADDRESS	1

Run a tape unit connected to Channel 0 control backward. The backward motion of a tape occurs when the tape spools are rotating in an anticlockwise direction and tape is being fed from the lower to the upper spool.

A TF order must not be followed by a TR order, or vice versa, since the forward drive may fail to disengage before the reverse drive engages so snapping the tape.

4.3.1.4 The Order TR1 (TAPE REVERSE)

34		18
17		1
1 1 0 1 1	NO ADDRESS	1

Run a tape unit connected to Channel 1 control backwards.

4.3.1.5 The Order TH0 (TAPE HALT)

34		18
17		1
1 1 1 0 0	NO ADDRESS	1

Stop a tape unit connected to Channel 0 control. This control
is absolute in that the tape will halt and restart if a TH
order is followed immediately by a TF order.

4.3.1.6 The order TH1 (TAPE HALT)

34		18
17		1
1 1 1 0 1	NO ADDRESS	1

Stop a tape unit connected to Channel 1 control.

4.3.1.7 The Order FG0 (FIND GAP)

34		18
17		1
0 1 1 0 0	NO ADDRESS	1

This order is only applicable when the tape is in motion, and
it affects only Channel 0 tape transport control and erase
orders. In operation it prevents these orders from being obeyed
until an erased section of tape, following words on the tape,
has been detected.

4.3.1.8 The Order FG1 (FIND GAP)

34		18
17		1
0 1 1 0 1	NO ADDRESS	1

As for FG0, except that the tape unit must be under Channel 1
control and Channel 1 tape transport and erase orders, only,
are affected.

4.3.2 Magnetic Tape Reading and Writing Orders

There are ten orders associated with the reading and
writing of information on tape. Five of these apply to Channel
0 control and five to Channel 1 control. Further, since each
tape unit has a separate reading and writing head, it is
possible to follow a writing order by a reading order without
the need to first reverse the direction of tape motion. Since
the input and output channels are independent, concurrent
reading and writing with different high speed store blocks and
tape units, is possible. It is not possible to read from tape
following a TR order.

4.3.2.1 The Order WT0 (WRITE on TAPE)

34		18
17		1
1 0 0 0 0	NO ADDRESS	1

Write a word from the upper half of the accumulator onto a
magnetic tape under Channel 0 control.

4.3.2.2 The Order WT1 (WRITE on TAPE)

34		18
17		1
1 0 0 0 1	NO ADDRESS	1

Write a word from the upper half of the accumulator onto a magnetic tape under Channel 1 control.

4.3.2.3 The Order RT0 (READ TAPE)

34		18
17		1
1 0 1 0 0	NO ADDRESS	1

Read the next word on a tape under Channel 0 control and add the word to the accumulator. Since the accumulator is used, 0-code orders will not be obeyed until this order is completed. The accumulator is not cleared before adding the word read to the accumulator.

4.3.2.4 The Order RT1 (READ TAPE)

34		18
17		1
1 0 1 0 1	NO ADDRESS	1

Read the next word on a tape under Channel 1 control.

4.3.2.5 The Order BT0 (BLOCK to TAPE)

34	29	26	18
17	12	9	1
1 0 0 1 0	BLOCK ADDRESS	NO ADDRESS	1

Write a block of 64 words from the high speed store block address specified onto magnetic tape under Channel 0 control. Any subsequent orders which do not involve high speed store block output will be performed during the transfer. Information in the block specified can still be addressed whilst this order is being obeyed, hence care must be taken not to overwrite this information before it has been transferred to tape.

4.3.2.6 The Order BT1 (BLOCK to TAPE)

34	29	26	18
17	12	9	1
1 0 0 1 1	BLOCK ADDRESS	NO ADDRESS	1

As for the order BT0 except that Channel 1 control is used.

4.3.2.7 The Order TB0 (TAPE to BLOCK)

34	29	26	18
17	12	9	1
1 0 1 1 0	BLOCK ADDRESS	NO ADDRESS	1

Transfer a block of 64 words from a tape under Channel 0
control to the block of high speed store specified. Any orders
not referring to locations in the block concerned will be
obeyed during the transfer. Those which do, and any high speed
store input orders, will not be obeyed until transfer is
completed.

4.3.2.8 The Order TB1 (TAPE to BLOCK)

34	29	26	18
17	12	9	1
1 0 1 1 1	BLOCK ADDRESS	NO ADDRESS	1

As for TB0 except that Channel 1 control is used.

4.3.2.9 The Order ET0 (ERASE TAPE)

34	18
17	1
1 1 1 1 0	NO ADDRESS	1

Erase a tape as long as it is in motion under Channel 0
control. The erasure will operate under both TF and TR orders
and will only cease after a TH order. Hence it is important
that a TH order be given at some point after an ET order before
attempting to rewind tape either under machine control or
manual control. It must be remembered that when an ET order
occurs, erasure is not immediate so that some noise will be
left on the tape. Under most circumstances this will be
ignored by the machine, the possible exception being that the
FG order which may find two gaps between blocks.

4.3.2.10 The Order ET1 (ERASE TAPE)

34	18
17	1
1 1 1 1 1	NO ADDRESS	1

As for ET0 except that Channel 1 control is used.

4.3.3 The Peripheral Equipment Switching Order

It has already been mentioned in paragraph 4 that the 1-
code orders contain a special order for switching control
between peripheral equipments of the same type. This facility
allows the connection of any number of paper tape readers,
punches and magnetic tape units to the machine as well as any
other type of unit of a similar nature. However, only two
paper tape readers, two paper tape punches and four magnetic
tape units are physically wired to the machine.

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4.3.3.1 The Order US (USE)

34	29	26	18
17	12	9	1

0 1 1 1 1	ADDRESS X	ADDRESS Y	1

Use the Control channel specified by address X to control the appropriate peripheral equipment whose unit number is specified by address Y. The available control channels are as follows:

Address X	Equipment Controlled
0	paper tape readers
1	paper tape punches
2	magnetic tape units Channel 0 control
3	magnetic tape units Channel 1 control

Thus, if the address X of a tape order is 2 and the address Y is 3, then the fourth tape unit will respond to all tape orders with zero addresses in a program.

5.   CODING FOR WREDAC

It has already been seen in the foregoing that the coding for WREDAC makes use of a two letter mnemonic to specify the function. The teletype equipment used for punching five hole paper tape has keyboards marked with the two letter mnemonic programming code. Further, the selecting bars are also arranged so as to cause the punching of the binary equivalent of the desired function on one row. Appendix V gives the complete list of teletype symbols with their equivalent meaning in machine function code. The punching of the address, B-line required, and code digit, is carried out in the following manner.

(a) Every 0-code order must terminate in one of the characters α, β, γ or δ.

(b) Every 1-code order must terminate in the character ϕ

(c) The address may be punched as

      (i)   An absolute decimal address
      (ii) An absolute decimal address giving the block reference and store reference within the block
      (iii) A relative address given by a specific letter
      (iv) A combination of the preceding three methods.

The method of setting the relative addressing facility, and the letters available is given in paragraph 6. The following examples will assist in the understanding of the coding method.

For 0 code orders, if FN stands for any two letter mnemonic, then write and punch

(i)	FN X	α	$0 <= X <= 511$
or (ii)	FN X/Z	α	$0 <= X <= 7, 0 <= Z <= 511 - X.2^6$
or (iii)	FN	Aα	where A has been previously set equal to X (see para.6)
or (iv)	FN X/Z	Aα	

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In general,

FN (X/Z A B D etc.) α

becomes

FN (X.2^6+Z+A+B+D+ etc.........)α

where

0 <= (X.2^6+Z+A+B+D+.......etc.) <= 511

if only the address is to be formed. Otherwise the relative address stores A, B, D, etc. may contain other functions as well as addresses, whence

FN (X/Z A B D etc.) α

becomes

(FN (X.2^6+Z)α) +(A) + (B) + ... etc.

For 1-code orders, the following applies

(d) For other tape orders (except FG) write and punch

FN   φ (for channel 0 control)
FN   1φ (for channel 1 control)

(e) For FG orders, write and punch

FG0   φ (for channel 0 control)
FG1   φ (for channel 1 control)

(f) For US orders write and punch

US X/Y φ
  0 <= X <= 7
  0 <= Y <= 255
however, at present, X <= 3 and Y <= 3.

As already noted in paragraph 2 above, two instructions can be contained in a single machine word. Hence, a pair of instructions will appear in a high speed store location as follows:

	ODD HALF				EVEN HALF			
34 30	29 21	20 19	18	17 13	12 4	3 2	1
FUNCTION	ADDRESS	B-LINE	CODE	FUNCTION	ADDRESS	B-LINE	CODE

Since the WREDAC is a serial machine, the least significant digit, (i.e. digit position 1) is always available in time before any of the remaining digits, and the even half of the word is always available before the odd half of the word. Hence, the order in the even half of the word is obeyed before the order in the odd half of the word. It is therefore convenient, when writing a program, to set down the order in the even half of the word first, followed by the order in the odd half of the word, on the same line. The reading of a program then follows as in normal reading, i.e. from left to right. The programming sheets are especially marked to assist with this convention as shown below, and the orders are punched as they appear on the programming sheet.

NO.	ORDERS	
	EVEN	ODD
0	CA 6 α	CL 10 α
1		
2		

Thus the order "CA 6 α" will be obeyed first, followed by the order "CL 10 α", but these orders will appear in the machine as:

ODD HALF WORD	EVEN HALF WORD

```
 1 0 0 1 1 0 0 0 0 1 0 1 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 0
        CL  10  α                              CA  6  α
```

Note that in writing orders, it is not possible to write and punch

<center>FN   (Address)   (α, β, γ, δ) ϕ</center>

e.g. CA X/Y δϕ is meaningless and will not appear in the machine as
written but as "CA X/Y δ" followed by "SE ......", so that all
succeeding orders will be incorrectly formed.

<center>### 6.   THE INPUT OF PROGRAM TO THE WREDAC</center>

In order to avoid the necessity for writing programs in absolute
binary format, the system of mnemonic coding described in paragraph 5 was
adopted. However, it is now necessary to place in the machine an
assembler-compiler routine which will transform the mnemonic code to
absolute binary code. In addition, it is desirable to have stored within
the machine a number of commonly used constants before a program
commences. The routine which performs the assembler-compiler operation
and sets up the stores with the constants is usually referred to as the
"Initial Orders". To avoid the need for preceding every program with a
set of Initial Orders in absolute binary, these Initial Orders are
permanently stored on track 0 of the disc. This track is made
inaccessible to transfers from the high speed store. The calling
sequence which brings these Initial Orders into the high speed store is
to set up on the number generator the orders:

<center>

Odd Half   Even Half

GE 8 α   DB   ϕ

</center>

and then to operate the manual transfer of control key, followed by a
single operation of the 'single shot' key when the 'step-by-step' key is
in the 'normal' position. The Initial Orders will then be transferred
from sector 0 of the disc to block 0 of the high speed store and entry to
the orders made at the order in the even half of location 8. The routine
will set the machine B-lines to group 0, counting on β, connect No.0
input and output paper tape equipments to the machine, and connect tape
unit No.0 to control channel 0 and tape unit No.1 to control channel 1.
The routine will then proceed to read characters from a paper tape
previously placed in the appropriate tape reader, assemble the tape
characters into absolute binary orders, and compile the tape orders into
a program.

6.1 Paper Tape Warning Characters
Two functions have been set aside in the 1-code orders to act as
warning characters for initiating action within the Initial Orders.
These functions are usually referred to as 'cues' and never appear in the
compiled machine program.

6.1.1 The Function QA
Immediately preceding every independent set of orders on paper
tape there must be an order of the form

<center>QA X ϕ ,   0 <= X <= 511</center>

There must be no blank tape between the 'ϕ' character and the
next function character, except, possibly, one CH character.

The effect of this warning cue is to cause the Initial Orders to
place the next order on the paper tape, when assembled, into the
even half of the high speed store address X, and successive orders
into

<center>X_o, $\overline{X+1_e}$, $\overline{X+1_o}$ . . . . . etc.</center>

Thus, the assembled orders will be compiled into a program
occupying the even and odd halves of high speed store addresses,
the first of which is address X.

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In addition, the Initial Orders will cause $X \times 2^{-12}$ to be stored
in the odd half of the high speed store address 7 for subsequent
reference (see paragraph 6.2 below).

6.1.2 The Function QC

At the end of a program tape it is necessary to direct the
machine control to some specific order in the program if it is to
commence automatic operation. The warning cue for this function is
an order of the form

<div align="center">QC ϕ</div>

punched at some point following the order on the tape after which
automatic operation of the tape program is desired.

Immediately following the 'QC ϕ' order there must be a transfer
of control order of the form

	CH	X	α
or	GE	X	α
or	PO	X	α
or	PE	X	α

Upon detecting the 'QC ϕ' order, the Initial Orders will cause
the following transfer of control order to be immediately obeyed,
without it being complied into the machine program.

6.2 Constants and Relative Address Locations

The machine high speed store addresses from 4 to 6 inclusive have been
reserved for certain constants which are part of the Initial Orders stored
on sector 0 of the disc. The addresses from 7 to 12 inclusive are reserved
for the temporary storage of relative addresses. The following table
indicates the constants available, and the teletape characters which are
valid relative addresses or 'preset parameters'. The Initial Orders, upon
detecting a preset parameter, cause the contents of that preset parameter
location to be added to the machine order being assembled. Since the
machine orders require only 17 digits, it is possible to have 11 preset
parameters in 5½ machine storage locations.

Location	ORDERS		Remarks
	EVEN	**ODD**	
0	Number	Generator	
1			B-Line 1
2			B-Line 2
3			B-Line 3
4	IF ϕ	CH α	equivalent to 2^{-32}
5	CH 1 α	CH α	equivalent to 2^{-29}
6	CA α	GE α	equivalent to $2^{-3}+2^{-16}$
7	Pseudo Order	A	These locations are used
8	B	D	for holding preset
9	G	H	parameters. Reference is
10	K	M	made to them by the
11	N	P	teletape character shown
12	S	W	

In order to set the parameter locations prior to reading in a
program, it is necessary to punch:

<div align="center">QA X ϕ   8 <= X <= 12</div>

followed by the desired settings in the form:

<div align="center">Function   Address   B-Line or terminator.</div>

Once a preset parameter location has been set it will remain set
until changed by the program following another QA X ϕ tape cue.
Hence, following the initial setting, a "QA" function can have a
relative address, i.e. it is possible to write

<div align="center">QA   Bϕ</div>

provided B has been previously set to some desired address X.

One order in the above table requires comment since it has been omitted from the list of effective orders. The function IF (INPUT FAST) is not used at present in the machine and has been reserved for future development of high speed input equipment. It will also be found that Appendix 5 has an order OF (OUTPUT FAST) which is complementary to IF and is not at present in use. The order IF has all zeros for its function digits, hence IF ϕ will be assembled as 2^{-16} or 2^{-32} depending on whether it is in an even or odd half of a word.

The preset parameter Y is also somewhat different from the other preset parameters, since it is fixed in value at 2^{-32} and occupies the even half of location 4. Its purpose is to allow for the formation of pseudo-orders (i.e. program constants) of the form

| Function | Address | B-Line Code |

e.g. instead of   CA X $\delta\phi$, which will not assemble correctly, write   CA X Yδ which has the same meaning and will assemble correctly.

It is also now possible to explain the use of the preset parameter A. Since the QA order causes the preset parameter location 7_o to be set with the address of the QA order, and since reference to any preset parameter in an address causes addition of the contents of the preset parameter location to the address of the order, the parameter A becomes a relative address for that section of the program headed by that particular QA order. Thus writing and punching:

QA   64 ϕ

NO.	Orders EVEN	Orders ODD	NOTES
0	CL α	IM	Clear Acc and input character
1	SR 10 α	CT 6 Aα	form CH x z in Acc
2	AE 6 Aα	CE 4 Aα	form AE x + 7A z
3	AO 5 Aα	CE 2 α	Put AEα in B-line γ
4	(CH α)	OM ϕ	Obey AE x + 7Az, output character
5	GE Aα	AE α	Return control
6	AE 7 Aα	CH 15 γ	Pseudo orders
7			Read Table
.			

as part of a program, would cause the machine to assemble the orders as if they had been written in the following form, commencing at location 64.

NO.	Orders EVEN	Orders ODD	NOTES
64	CL α	IM ϕ	
65	SR 10 α	CT 70 α	
66	AE 70 α	CE 68 α	
67	AO 69 α	CE 2 α	
68	(CH α)	OM ϕ	
69	GE 64 α	AE α	
70	AE 71 α	CH 15 γ	
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(Note that this is not a workable program since it has no proper entry or exit point and is longer than necessary; it has been written in this form for simplicity of illustration).

The coding example given above also illustrates some other features which may be usefully noted. The basis of the program is to transform a character on teletape in one code to a second code and output the new character to the punch. The method employed here is one of table look-up. The 32 possible characters are stored in the odd and even halves of locations 71 to 86 inclusive. When an input character has a 1 in its least

significant position, the order in (4A)$_e$ will be "AE x +7A γ" and since γ
is set with "AE α" this order will become "A0 x + 7Aα". If the least
significant digit of a character is zero, the order will remain as "AE x +
7A α". The second point to note is that the assembled order "AE x + 7A z"
is cleared to the even half of location 4A. This is an x (mod 4) location,
(x = 0), outside of the immediate range of the four locations containing
the "CE 4 Aα" order. The reason for ensuring that this is carried out when
modifying orders in a sequence will be treated in more detail in paragraph
7.

7.   THE TIMING OF MACHINE OPERATIONS

   The timing of machine operations is extremely complex due to the fact that
four-word delay lines are used within the high speed store, and eight orders are
brought into the order store each time it requires filling. In addition, control
transfer orders cause a refilling of the order store each time they are effective.

7.1   Timing of 0-code orders

   The first point to note is that orders already transferred to the order
store cannot be modified except through a B-line, before being obeyed. As a
result, order modification must occur as in the previous coding example, i.e.
outside the present set of eight orders in the order store, or a transfer of
control order must be obeyed at some point following the order modification but
preceding its operation. Thus we may write:

```
          EVEN           ODD

     0    AE      Bα      AO  2  Aα
     1    CE  2  Aα      PE  2  Aα
     2    (CH      α)    CA      α
```

   However, it is quite clear that fastest operation will be obtained if the
control transfer order is avoided and the method adopted in the example of
paragraph 6 above employed.

   Also arising from the method of order store refilling, faster operation will
result when any transfer of control order immediately precedes a 0(mod 4)
address and transfers control to a 0(mod 4) or 3(mod 4).

   Again, the arithmetic operations of multiplication and division can operate
concurrently with the refilling of the order store. Hence if a multiplication
or division order (i.e. the orders MA, MS, LD) are placed in the odd half of a
3(mod 4) location, the order store refill will proceed during the operation of
the arithmetic order, thus greatly reducing the time for multiplication and
division in conjunction with an order store refill.

   Since four words are stored sequentially in one machine delay line, it is
possible to get a further reduction in order operating time by always following
an x(mod 4) address in an order with an X+1(mod 4) address in the following
order, except when an order store refill takes place between the two orders, or
when B-line modification is involved. The optimum addresses are an x(mod 4)
value followed by an x+1, x+2, or x+3(mod 4) value, when an order store refill
intervenes between the two orders and an x(mod 4) followed by an (x+2)(mod 4)
with a B-line modification.

7.2 Timing of 1-code orders for Disc Transfers
   The magnetic disc rotates at 2,300 revolutions per minute so that four
sectors pass under a given head in approximately 26 milliseconds. Upon
receiving a disc transfer order, the control unit will wait until a 'beginning
of sector' signal occurs, following which it will compare the two least
significant sector address digits with similar digits on a disc 'clock' track.
Upon obtaining agreement, the following disc sector will be transferred to the
high speed store in 6.5 milliseconds. When transferring a number of sectors
to high speed store, the optimum timing is obtained with addresses in the
cyclic order 3, 2, 1, 0(mod 4)

7.3 Timing of 1-Code Orders for Input/Output and Magnetic Tape Units.

The timing of 1-code orders is in general, determined by the time taken to operate electro-mechanical equipment. The maximum speed of the photo-electric reader is 200 characters/second and of the present punch 25 characters/second. The stop/start time of the magnetic tape units is less than 5 milliseconds in each case, and the running speed is 75″ *(inches)*/second.

With all orders for writing on magnetic tape, the method employed is to bias to magnetic saturation in either of the two possible directions, and the bias direction for zeros is equivalent to an erasure of the tape. Hence the use of the ET order can cause a mark to appear on the tape, and this mark can cause two erased sections of tape to be detected by the FG order when searching in a reverse direction. The ET order operates immediately after it is set up in the machine.

Following a WT order the word written on the tape occupies 0.5 milliseconds of magnetic tape or 0.038″ of tape. There will be a minimum gap of 0.3 milliseconds between single words written on magnetic tape. A block written on the tape by the BT order occupies 32.64 milliseconds of the tape time or 2.45″ of tape.

The FG order will not detect an erased section of tape which is less than 1.0 milliseconds of tape time or 0.075″ of tape.

There is an important control signal or "suppression" employed with tape reading orders. This suppression is frequently referred to as the 'J-suppression'. If sufficient data cannot be found on a tape in order to satisfy the control requirements of these orders, the suppressions may be cleared and the tape transports halted by depression of the 'J' reset key. Note that a program error can cause the J-suppression to be activated even though the tape units are not in use.

The magnetic tape transport orders (TF, TR, TH and ET), have certain deliberate delays associated with their operation which prevent the machine from proceeding to the next associated tape order for some specified time. These delays are

TF orders	7 milliseconds
TR "	7 "
TH "	7 "
ET "	7 "

Note, however, that the ET delay is concurrent with the preceding TF delay.

8.   SPECIAL MACHINE FEATURES

There are some special features associated with the WREDAC. Two of these are concerned with program debugging and two with magnetic tape operation. The debugging aids are associated with the machine console and provide a means for stopping the machine on any desired 0-code order together with a complete display of the high speed store and the machine working stores. One of the special magnetic tape facilities allows words of variable length to be put into the machine, the other concerns the type of read/write head employed.

8.1 The Flying Stop and Console Display.

The machine console has, in addition to the number generator, a set of 14 keys which when set with the function and address of a machine order will cause the automatic operation of the machine to stop if a third key (the 'op.stop' key) is set up. This facility is only available on 0-code orders. Further, 0-code orders under B-line modification require the flying stop keys to be set to the order resulting from the modification. In operation, the order set on the flying stop keys is obeyed before the machine halts, and the facility provides a rapid method for program debugging without the need to write special orders into a program.

The console display provides in one part a scan, in sets of 32 words, of the 512 words of the high speed store. A second part provides a scan of all machine working delay lines. In particular, the order register, order store, accumulator, R register, and all B-lines, are available for immediate inspection.

8.2 Variable Word Length Reading of Magnetic Tapes

The method of recording information on magnetic tape is series-parallel in nature. Six rows, each of six digits, form a normal tape word, although only 34 of these digits are effective, i.e. the machine reads six rows and ignores the two least significant digits in the least significant row.

Under certain circumstances, data may be recorded on magnetic tape with less than six rows to a data word. In these cases the machine will place a single data word in the most significant part of a machine high speed store location.

8.3 Magnetic Tape Read/Write Heads

The magnetic tape units are fitted with separate reading and writing heads, and it is possible to follow a writing order immediately by a reading order. There is, however, a time separation of 5 milliseconds between the writing head and the reading head, and the writing head effectively precedes the reading head. This facility allows the checking of information being written on magnetic tape without the need to halt the tape and reverse to the beginning of the information written.

REFERENCES

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2.   "   "   "   An Introduction to Programming for
                              Automatic Digital Computers. WRE TM 50

3.   Fenna D.   WREDAC Programming Memo No.8
                              New WREDAC initial Orders

4.   Bowie J.R.   WREDAC Programming Memo No.10
                              Multiple B-lines.

5.   "   WREDAC Programming Memo No. 3

6.   Main P.G.   WREDAC Programming memo No. 7

7.   Allen-Ovenstone J.   WREDAC Operating Memo. No. 3

8.   Bowie J.R.   WREDAC Operating Memo No. 5

APPENDIX I ABBREVIATIONS USED

Abbreviation	Equivalent
A	The storage locations whose address A is given by the address digits of the order.
(A)	The contents of the storage location given by the address A.
A_e	The even part (least significant half) of the location specified by the address A.
A_o	The odd part (most significant half) of the location specified by the address A.
(A_e)	The contents of the even half of the location specified by the address A, i.e. the least significant half of the word.
(A_o)	The contents of the odd half of the location specified by the address A, i.e. the most significant half of the word.
Acc	The double length accumulator.
(Acc)	The 68 bit contents of the double length accumulator.
R	The multiplier register.
(R)	The 34 bit contents of the multiplier register.
$\alpha,\ \beta,\ \gamma,\ \delta$	The B-lines 0, 1, 2, 3 respectively, i.e. the even parts of the high-speed store locations 0, 1, 2, 3.
$(\alpha),(\beta),(\gamma),(\delta)$	The contents of B-lines 0, 1, 2, 3 respectively.
l.s. & m.s.	Least significant and most significant respectively.
Block	Any of the eight 64-word blocks of the high-speed store.
Sector	Any of the 256 64-word sectors of the magnetic disc store.
Tape or Tape unit	Any of the magnetic tape input and output (Ancillary Stores).
Teletape	The five-hole teletype tape used as input and output.

The extensions of the abbreviations are obvious; thus (Acc_o) means the contents of the most significant half of the accumulator, and so on.

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APPENDIX II

The arithmetic and logical orders at present available on the WREDAC are:

NO.	Function Digits Binary	Tele-printer	Mnemonic Code	Description
0	00000	θ	CH	CHECK: Obey the order in A_0 if address of order is not zero and (Acc)=0
1	00001	A	GE	GO EVEN: Obey the order in A_e.
2	00010	B	PO	POSITIVE ODD: Obey the order in A_0 if (Acc) >= 0.
3	00011	C	PE	POSITIVE EVEN: Obey the order in A_e if (Acc) >= 0.
4	00100	D	NO	NEGATIVE ODD: Obey the order in A_0 if (Acc) < 0.
5	00101	E	NE	NEGATIVE EVEN: Obey the order in A_e if (Acc) < 0.
6	00110	F	JO	JUMP ODD: If (B-line) not= 0, obey the order in A_0; otherwise proceed serially. In both cases, add 1×2^{-29} to (B-line).
7	00111	G	JE	JUMP EVEN: If (B-line) not= 0, obey the order in Ae; otherwise proceed serially. In both cases, add 1×2^{-29} to (B-line).
8	01000	H	LD	LONG DIVISION: Divide (A) by (R) and add result to (Acc).
9	01001	I	SM	SET MULTIPLIER: Write (A) in the multiplier register.
10	01010	J	MA	MULTIPLY AND ADD: Multiply (A) by (R) and add result to (Acc).
11	01011	K	MS	MULTIPLY AND SUBTRACT: Multiply (A) by (R) and subtract result from (Acc).
12	01100	L	SL	SHIFT LEFT: Multiply (Acc) by 2^n where n = A.
13	01101	M	SR	SHIFT RIGHT: Divide (Acc) by 2^n where n = A.
14	01110	N	NM	NORMALISE: Multiply (Acc) by 2^n such that 1<= |(Acc)|<2 and write $n \times 2^{-29}$ (n>=0) in the selected B-line.
15	01111	O	MD	MODULISE: Replace (Acc) by its modulus.
16	10000	P	CA	CLEAR AND ADD: Clear Acc and add (A) to (Acc).
17	10001	Q	CS	CLEAR AND SUBTRACT: Clear Acc and subtract (A) from (Acc).
18	10010	R	SW	SWAP: Place (Acc) in A and (A) in Acc.
19	10011	S	CL	CLEAR: Write (Acc) in A and clear Acc.

NO.	Function Digits Binary	Tele-printer	Mnemonic Code	Description
20	10100	T	AD	ADD: Add (A) to (Acc).
21	10101	U	SA	SUBTRACT and ADD: Subtract (a) from (Acc)
22	10110	V	CT	COLLATE: Compare (A) and (Acc) and write 1 in the Acc where there is a 1 in both digit positions of both numbers.
*23	10111	W	UL	USE LOGIC: Switch the machine to the logic specified by A.
24	11000	X	SB	SET B line: Write in the B-line specified by the UL order $n \times 2^{-29}$ where n=A and $0 <= A <= 256$, or $-(n \times 2^{-29})$ when $512 - |n| \; \unicode{x22F9} \; A$ and $256 <= A <= 511$.
25	11001	Y	CO	CLEAR to ODD: Write (Acc_0) to A_0 and clear whole Acc.
26	11010	Z	CE	CLEAR to EVEN: Write (Acc) to A_e and clear whole Acc.
27	11011	α	ST	STORE: Write (Acc) in A and leave (Acc) unchanged.
28	11100	β	AO	ADD ODD: Add (A_0) to (Acc_0).
29	11101	γ	SO	SUBTRACT ODD: Subtract (A_0) from (Acc_0).
30	11110	δ	AE	ADD EVEN: Add (A_e) to (Acc_0).
31	11111	φ	SE	SUBTRACT EVEN: Subtract (A_e) from (Acc_0).

* See Appendix IV for details of addresses available with this order.

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APPENDIX III

The transfer (or 1–Code) orders available are:

NO.	Transfer Function digits Binary	Teleprinter	Mnemonic Code	Description
0	00000	θ	IF	INPUT FAST: Spare at present
1	00001	A	OF	OUTPUT FAST: Spare at present
2	00010	B	IL	INPUT to LEAST: Read row of teletape and add to 5 l.s. digits of upper half of (Acc)
3	00011	C	IM	INPUT to MOST: Read row of teletape and add to 5 m.s. digits of upper half of (Acc)
4	00100	D	OL	OUTPUT from LEAST: Punch on teletape 5 l.s. digits of upper half of (Acc)
5	00101	E	OM	OUTPUT from MOST: Punch on teletape 5 m.s. digits of (Acc)
6	00110	F	BD	BLOCK to DISC: Transfer a block to a sector
7	00111	G	DB	DISC to BLOCK: Transfer a disc sector to a block
8	01000	H		Spare
9	01001	I		Spare
10	01010	J		Spare
11	01011	K		Spare
12	01100	L	FG0	FIND GAP. Suppress all following tape orders referring to control channel 0 until an erased section of tape is found.
13	01101	M	FG1	FIND GAP. As for 12 but for orders referring to control channel 1
14	01110	N		Spare
15	01111	O	US	USE: Use peripheral equipment y with control channel x. x,y are given by address x/y.
16	10000	P	*WT0	WRITE on TAPE: Write (Acc) on a tape using channel 0 control
17	10001	Q	WT1	WRITE on TAPE: Write (Acc) on a tape using channel 1 control
18	10010	R	*BT0	BLOCK to TAPE: Transfer a block to a tape using channel 0 control
19	10011	S	BT1	BLOCK to TAPE: Transfer a block to a tape using channel 1 control
20	10100	T	*RT0	READ TAPE: Read next word on a tape using channel 0 control and add to (Acc)

| NO. | Transfer Function digits | | Mnemonic | |
	Binary	Teleprinter	Code	Description
21	10101	U	RT1	READ TAPE: Read next word on a tape using channel 1 control and add to (Acc).
22	10110	V	*TB0	TAPE to BLOCK: Transfer 64 words to a block from a tape using channel 0 control.
23	10111	W	TB1	TAPE to BLOCK: Transfer 64 words to a block from a tape using channel 1 control.
24	11000	X	*TF0	TAPE FORWARD: Run a tape connected to channel 0 control forward.
25	11001	Y	TF1	TAPE FORWARD: Run a tape connected to channel 1 control forward.
26	11010	Z	*TR0	TAPE REVERSE: Run a tape connected to channel 0 control backward.
27	11011	α	TR1	TAPE REVERSE: Run a tape connected to channel 1 control backward.
28	11100	β	*TH0	TAPE HALT: Stop a tape unit connected to channel 0 control.
29	11101	γ	TH1	TAPE HALT: Stop a tape unit connected to channel 1 control.
30	11110	δ	*ET0	ERASE TAPE: Write erase on a tape using channel 0 control.
31	11111	φ	ET1	ERASE TAPE: Write erase on a tape using channel 1 control.

SPECIAL NOTE: Only the mnemonic code symbols not marked by an asterisk are
                     punched for magnetic tape orders using the corresponding
                     telecode symbols. The address of 1 will then distinguish
                     between channel 0 and channel 1, e.g.

                          Punch TF   φ for TF0
                                 TF   1φ for TF1

                     The exception to this rule is the FG0, FG1 orders which
                     must be punched as FG0 φ   FG1 φ respectively.

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APPENDIX IV

MULTIPLE B-LINES

STRUCTURE OF THE UL ORDER CONCERNING B-LINES

The UL 1/x(α) order is the one which selects the group of B-lines and determines the disposition of the various facilities among the B-lines of the group. The **x** above signifies the combination of the 6 less significant digits of the address and (α) signifies any 0 code terminating character i.e. B-line modification of these UL orders still applies. In the case of a modification of these orders, modification is as specified by the previous UL order for B-lines.

The notation for the digits specified by **x** above involves the consideration of these digits as three pairs of digits. In descending order in significance of address digits A, B and C these pairs represent

    A   Addition of B-lines in order modification

        0 signifies order modification only by the contents of even half of the B-line designated.

        1 signifies that orders where β appears are to be modified by the sum of the contents of the even halves of locations 1 and 2.

        2 signifies that orders where γ appears are to be modified by the sum of the contents of the even halves of locations 2 and 3.

        3 signifies that orders where δ appears are to be modified by the sum of the contents of the even halves of locations 3 and 1.

In each case the terminating characters not mentioned cause the modification only by the contents of the even half of the B-line designated.

The sum of the contents of the B-lines is only that obtained from the address and function digits; less significant digits or carries developed therefrom do not appear.

    B   Group of B-lines

        These digits specify which group (0, 1, 2 or 3) of B-lines is to be used to occupy locations 1, 2 and 3.

    C   Allocation of Facilities Within Group

        These digits specify which location 1, 2 or 3 is to be provided with the SB, JO, etc. facilities.
        It will be noted that when these digits are both 0 these facilities are not available on any B-line.

NOTES:
1) The selection of a particular B-line implies the selection of the 3 B-lines to be used in the H.S.S.

2) When a B-line is not selected it retains the contents it had immediately prior to the last UIL order thereby providing extra storage.

3) Only 3 B-lines appear as H.S.S. locations on the left hand display. However all 12 appear on the right hand display.

4) The B-lines in use are unaffected by DB and TB orders.

5) The initial orders set the B-lines to 1 having the facilities, i.e. UL1/1α occurs explicitly in the initial orders on original entry.

6) On first approach to the machine no assumptions can be made about the B-line setting so that care must be taken if orders are to be obeyed without using the initial orders.

The following table may assist in the specifications of the UL1/x order on program sheets

	COUNTING FACILITY		ADDITIVITY			
1	2	3	4	5	6	7
SET	LOCN.	REF.	NONE	β	γ	δ
0	0		0	16	32	48
	1	β	1	17	33	49
	2	γ	2	18	34	50
	3	δ	3	19	35	51
1	0		4	20	36	52
	1	β	5	21	37	53
	2	γ	6	22	38	54
	3	δ	7	23	39	55
2	0		8	24	40	56
	1	β	9	25	41	57
	2	γ	10	26	42	58
	3	δ	11	27	43	59
3	0		12	28	44	60
	1	β	13	29	45	61
	2	γ	14	30	46	62
	3	δ	15	31	47	63

The numbers on the right are those corresponding to the digits above.

Column 1 corresponds to the group of B-lines selected, column 2 to the locations occupied in the high speed store. Column 3 shows the terminating character corresponding to the B-line having the SB, J0 etc. facilities. Column 4 shows the addresses which correspond to columns 1, 2 and 3 where the additive modifications facility is not required. Columns 5, 6 and 7 are as for column 4 except that these correspond to the conditions 1, 2 and 3 under A above.

EXAMPLE:
1. If it were desired to use group 2 of B-lines with the SB, J0 etc. facilities on location 2 the terminating character γ was to cause the order to be modified by the sum of contents 2 and 3 reference to line 13 and column 6 shows that the required order is UL1/42 α.

2. If the first 6 B-lines are holding information and it is desired to use a counting loop which does not disturb this information the order UL1/9α could be used. Reference to line 12 above shows that the counting facility is applied to the location to which β applies, and since 9 occurs in column 4 modification is only by the contents of the B-line specified by the terminating character. Further, since this occurs in group 2 none of the 6 B-lines containing information are available to the machine while the effect of this order continues.

APPENDIX V

Teleprinter Code   The keyboards of the various teletape equipments contain the following codes:

Punched in Binary	Decimal Equivalent	Letter Shift Teleprint	Function	Figure Shift Teleprint	Function
00000	0	θ (no effect)	CH	θ (no effect)	IF
00001	1	A	GE	. (Dec.pt)	OF
00010	2	B	PO	*	IL
00011	3	C	PE	1	IM
00100	4	D	NO	=	OL
00101	5	E	NE	2	OM
00110	6	F	JO	3	BD
00111	7	G	JE	;	DB
01000	8	H	LD	. (Full stop)	
01001	9	I	SM	4	
01010	10	J	MA	5	
01011	11	K	MS	:	
01100	12	L	SL	6	FG0
01101	13	M	SR	%	FG1
01110	14	N	NM	;	
01111	15	O	MD	(	US
10000	16	P	CA	−	
10001	17	Q	CS	7	WT
10010	18	R	SW	8	
10011	19	S	CL	?	BT
10100	20	T	AD	9	
10101	21	U	SA	/	RT
10110	22	V	CT	+	QA
10111	23	W	UL	)	TB
11000	24	X	SB	0	
11001	25	Y	CO	£	TF
11010	26	Z	CE	@	QC
11011	27	α (figure shift)	ST	α (figure shift)	TR
11100	28	β (space)	AO	β (space)	
11101	29	γ (carriage return)	SO	γ (carriage return)	TH
11110	30	δ (line feed)	AE	δ (line feed)	
11111	31	φ (letter shift)	SE	φ (letter shift)	ET

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